DESIGN NOTES

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DC Accurate Filter Eases PLL Design

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The LTC1062 is a versatile, DC accurate, instrumentation lowpass filter with gain and phase that closely approximate a 5th order Butterworth filter. The LTC1062 is quite different from presently available lowpass switched capacitor filters because it uses an external (R, C) to isolate the IC from the input signal DC path, thus providing DC accuracy. The DC accurate output, pin 7 of Figure 1, is buffered by an internal op amp from the switched capacitor network. The output of the switched capacitor network drives the bottom of C1. The input and output appear across an external resistor and, the IC part of the overall filter handles only the AC path of the signal. A buffered output is also provided (Figure 1) and its maximum guaranteed offset voltage over temperature is 20mV. Typically the buffered output offset is 0-5mV and drift is 1μV/°C. The use of an input (R, C) also provides other advantages, such as lower noise and antialiasing.

With commercially available PLLs, the loop filter is designed by the user to optimize the loop performance. For a variety of applications, a 1st or 2nd order lowpass passive or active R, C filter will do the job. When minimum output jitter and good transient response are required simultaneously, the design of the loop filter becomes more sophisticated. For instance, a fast transient response implies wide filter bandwidth and a reduced VCO output jitter implies minimum ripple at the VCO input. This is achieved by high outband attenuation of the lowpass filter. The LTC1062 provides the above requirements as well as economy and cutoff frequency programmability to be used advantageously in PLL designs.

The circuit of Figure 2 illustrates the use of the LTC1062 as a loop filter. The power supplies for the circuit are a single 5V

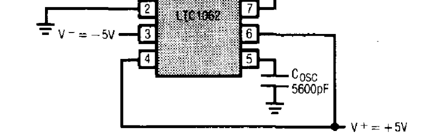


Figure 1. 8Hz 5th Order Butterworth Lowpass Filter

for the PLL and ±5V for the LTC1062. The CMOS PLL is a CD4046B. The LTC1062 can also be used with a single 5V with some additional level shifting (see AN20). Phase detector #2 drives a diode-resistor limiter combination to make the voltage at input R of the LTC1062 swing from one diode above ground to one diode below the 5V supply. Additionally, the two 5k resistors establish a maximum AC impedance to keep the LTC1062 in its operating region and to bias the VCO input at its mid point when phase detector #2 switches into a three-state mode.

An empirical design procedure for input frequencies less than 5kHz ($f_{IN} \leq$ 5kHz, Figure 2) is illustrated below:

- Given the minimum input frequency value, the cutoff frequency, f_C, of the LTC1062 should be chosen as:

  $$1/6\,(f_{IN(MIN)}) \leq f_C \leq 1/4\,(f_{IN(MIN)})$$

  The internal (or external) clock frequency of the LTC1062 should be 150 to 250 times the desired cutoff frequency, f_C.

- The capacitor C_{OSC} setting the LTC1062's internal oscillator should be chosen by:

  $$C_{OSC} = \left(\frac{130\text{kHz}}{250 \times f_C} - 1\right) \times 33\text{pF}$$

  By further decreasing the value of C_{OSC}, the internal clock frequency of the LTC1062 increases and the damping of the loop also increases.

- By letting the value of C = 0.047μF, the LTC1062 input resistor R should be:

  $$R \simeq \frac{5500\text{k}\Omega}{f_C\,(\text{Hz})}$$

  Note: For this application, the loop filter is not required to be maximum flat and, therefore, the (R, C) values of the LTC1062 can be within ±5% tolerance.

To illustrate the performance difference between a lowpass passive R, C loop filter and the LTC1062, the circuit of Figure 2 was tested for a PLL with a 60Hz ±10% input fre-

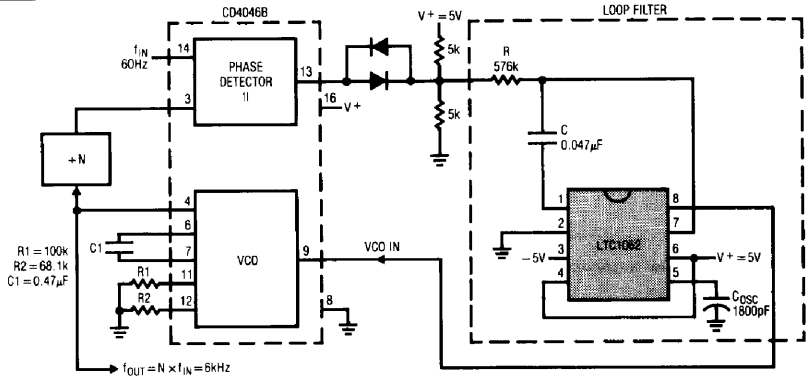
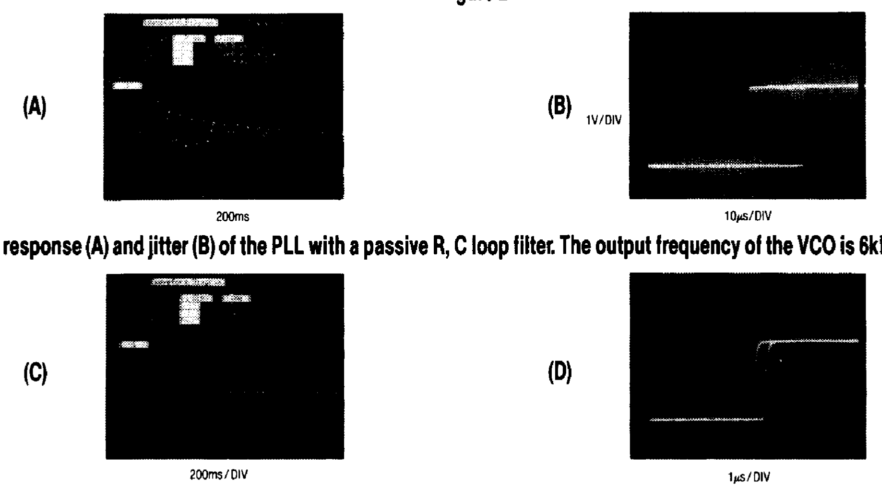


Figure 2



Transient response (A) and jitter (B) of the PLL with a passive R, C loop filter. The output frequency of the VCO is 6kHz and the ÷ N = 100.

Transient response (C) and jitter (D) of the PLL with the LTC1062 used as a loop filter. The VCO output frequency is 6kHz and the ÷ N = 100. The jitter is reduced to the internal jitter of the VCO.

Figure 3

quency range and with ÷N = 100. Then, the PLL's VCO output could be used to drive the clock input of a precision switched capacitor filter, such as an LTC1060A set up in a 100:1 clock to center ratio, and configured as a 60Hz sharp notch or bandpass filter. Figure 3A shows the transient response of the loop when a passive R,C loop filter, Figure 4, is used. The input frequency is shifted from 54Hz to 60Hz and the loop takes 820ms to settle within 5% of its steady stable value. The corner frequency of the R, C passive filter is 22Hz. The natural frequency of the loop is approximately 10Hz and the damping factor less than 0.1. Figure 3B shows the jitter at the VCO output under the above conditions. A 30µs jitter with f_{OUT} = 6kHz corresponds to 18% instantaneous frequency inaccuracy. This makes the PLL VCO output unusable as a

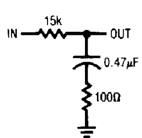


Figure 4. Lowpass R, C Filters used for PLL Example

clock generator for a tracking switched capacitor filter. A small improvement in the VCO output jitter could be achieved by further decreasing the filter's cutoff frequency; this, however, would further penalize the circuit's settling time.

Figures 3C and 3D show the PLL performance when an LTC1062 is used as a loop filter. The corner frequency f_C of the LTC1062 was set at 9.5Hz (≈ 1/6 f_{IN}) and its internal clock was set for 2.4kHz (≈ 252 x f_C). The settling time of the loop was 320ms and the damping factor was optimally set to 0.7. The 1µs VCO output jitter, f_{OUT} = 6kHz, was measured over 5 periods and it is attributed to the inherited jitter of the VCO internal circuitry. With the LTC1062 used as a loop filter, the circuit's jitter corresponds to 0.12% frequency error. This is quite adequate to drive the clock input of 0.3% accurate switched capacitor filters, such as LTC1059A or LTC1060A.

For Filter literature call **800-637-5545**. For help with an application call (408) 432-1900, Ext. 361.